01-19-00 A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Kie Y. Ahn et al.

Title: METHODS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS

Attorney Docket No.: 303.648US1

PATENT APPLICATION TRANSMITTAL

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items and information (as indicated with an "X"):

- X Utility Patent Application under 37 CFR § 1.53(b) comprising:
  - X Specification (24 pgs, including claims numbered 1 through 42 and a 1 page Abstract).
  - X Formal Drawing(s) (3 sheets).
  - X Signed Declaration (3 pgs).
  - X Signed Power of Attorney (1 pg.)
  - X Check in the amount of $2,178.00 to pay the filing fee.
- X Assignment of the invention to Micron Technology, Inc. (3 pgs) and Recordation Form Cover Sheet.
- X Check in the amount of $40.00 to pay the Assignment recording fee.
- X Return postcard.
- ☐ The filing fee has been calculated below as follows:

	No. Filed	No. Extra	Rate	Fee
TOTAL CLAIMS	42 - 20 =	22	x 18 =	$396.00
INDEPENDENT CLAIMS	17 - 3 =	14	x 78 =	$1,092.00
[ ] MULTIPLE DEPENDENT CLAIMS PRESENTED				$0.00
BASIC FEE				$690.00
TOTAL				$2,178.00

Please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

By: _____
Atty: Eduardo E. Drake
Reg. No. 40,594

Customer Number 21186

"Express Mail" mailing label number: EL254616856US Date of Deposit: January 18, 2000

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

By: Shawn L. Hise

Signature: _____

METHODS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS

Technical Field

The present invention concerns methods of semiconductor device or integrated circuit manufacturing, particularly methods of forming interconnects from copper and other metals.

Background of the Invention

Integrated circuits, the key components in thousands of electronic and computer products, are interconnected networks of electrical components fabricated on a common foundation, or substrate. Fabricators typically use various techniques, such as layering, doping, masking, and etching, to build thousands and even millions of microscopic resistors, transistors, and other electrical components on a silicon substrate, known as a wafer. The components are then wired, or interconnected, together with aluminum wires to define a specific electric circuit, such as a computer memory. The aluminum wires are typically about one micron thick, or about 100 times thinner than a human hair.

To form the aluminum wires, fabricators sometimes use a dual-damascene metallization technique, which takes its name from the ancient Damascan metalworking art of inlaying metal in grooves or channels to form ornamental patterns. The dual-damascene technique entails covering the components on a wafer with an insulative layer of silicon dioxide, etching small holes in the insulative layer to expose portions of the components underneath, and subsequently etching shallow trenches from hole to hole to define a wiring pattern.

Etching the trenches and holes entails forming a mask, using photolithographic techniques, on the insulative layer. The masks, which typically consists of a material called photoresist, shields some portions of the insulative layer from the etchant and allows the etchant to dissolve away other portions. After etching, fabricators remove the mask to expose the patterned insulative layer. They then blanket the entire insulative layer with a thin sheet of aluminum and polish off

the excess, leaving behind aluminum vias, or contact plugs, in the holes and thin aluminum wires in the trenches.

The complexity of some integrated circuits demand several interconnected levels of wiring. Some circuits, such as microprocessors, have five or six interconnected levels, with each level formed by repeating the basic dual-damascene produce. For example, to form a second wiring level, fabricators apply a new insulative layer over the first wiring layer, form another mask on the new layer, etch holes and trenches into the new layer, remove the mask, blanket the new layer with aluminum, before finally polishing off the excess to complete it.

In recent years, researchers have begun using copper instead of aluminum to form integrated-circuit wiring, because copper offers lower electrical resistance and better reliability at smaller dimensions. Fabrication of copper-wired integrated circuits sometimes follows an extension of the dual-damascene method which includes an additional step of lining the holes and trenches of an insulative layer with a copper-diffusion barrier before blanketing the layer with copper and polishing off the excess. (The diffusion barrier is generally necessary because copper atoms readily diffuse through common insulators, such as silicon dioxide, resulting in unreliable or inoperative integrated circuits.) Typically, the copper-diffusion barrier is more than 30 nanometers thick and consists of tantalum, tantalum nitride, tantalum-silicon-nitride, titanium nitride, or tungsten nitride. Filling the barrier-lined holes and trenches with copper generally entails depositing a thin copper seed layer on the copper-diffusion barrier, electroplating copper on the seed layer, and then polishing off the excess.

The present inventors identified at least two problems with using the extended dual-damascene technique for making the copper wiring. The first is that typical copper-diffusion barriers add appreciable resistance to the copper wiring, and thus negate some promised performance advantages. And, the second is that the number of separate procedures or steps necessary to make the copper wiring using the extended technique makes fabrication both costly and time consuming.

Accordingly, there is a need for better ways of making copper wiring for integrated circuits.

Summary of the Invention

To address these and other needs, the inventors devised unique methods of forming wiring from copper and other desirable metals, some of which allow fabrication of copper wiring with fewer steps and lower electrical resistance than some conventional methods. One exemplary method forms a first mask layer with openings that expose underlying transistor contact regions and then forms on the first mask layer a first metal structure of for example, copper, silver, or gold-based metals, which contacts the transistor contact regions. Next, with the first mask layer still in place, the exemplary method forms a second mask layer with openings that expose portions of the underlying first metal structure and then forms on the second mask structure a second metal structure which contacts exposed portions of the first metal structure.

After formation of these mask layers and metal structures, the exemplary method removes both mask layers in a single removal procedure, leaving a space around and between the metal structures. The first and second metal structures are then coated in a single procedure with a 6-10-nanometer-thick diffusion barrier, such as WSi_xN_y (tungsten-silicon-nitrogen.) And subsequently, the space is filled, in another single procedure, with one or more insulative materials, such as silicon dioxide, an aerogel, or an xerogel.

Brief Description of the Drawings

Figure 1 is a cross-sectional view of an exemplary integrated-circuit assembly 100, including two transistors 214a and 214b and a mask layer 216 with via holes 216a and 216b, and a trench 216c;

Figure 2 is a cross-sectional view of the Figure 1 assembly after formation of conductive structure 218 within holes 216a and 216b and trench 216c;

Figure 3 is a cross-sectional view of the Figure 2 integrated-circuit assembly after formation of a mask layer 220 on conductive structure 218;

Figure 4 is a cross-sectional view of the Figure 3 assembly after formation of a conductive structure 222 on mask layer 220;

Figure 5 is a cross-sectional view of the Figure 4 assembly after removal of mask layers 116 and 220 to define space 224;

Figure 6 is a cross-sectional view of the Figure 5 assembly after forming a diffusion-barrier 226 on conductive structures 218 and 222;

Figure 7 is a cross-sectional view of the Figure 6 assembly after filling space 224 with one or more insulative materials to form a two-level insulative structure 228;

Figure 8 is a block diagram of an exemplary integrated memory circuit which incorporates the present invention.

Description of the Preferred Embodiments

The following detailed description, which references and incorporates Figures 1-8, describes and illustrates specific embodiments of the invention. These embodiments, offered not to limit but only to exemplify and teach the concepts of the invention, are shown and described in sufficient detail to enable those skilled in the art to implement or practice the invention. Thus, where appropriate to avoid obscuring the invention, the description may omit certain information known to those of skill in the art.

Figures 1-7 show a number of cross-sectional views of a partial integrated-circuits assembly 100, which taken collectively and sequentially, illustrate a unique exemplary method of making integrated circuits, and more particularly making integrated-circuit wiring in accord with teachings of the present invention. The method, as shown in Figure 1, begins with a known integrated-circuit assembly or structure 100, which can exist within any integrated circuit, a dynamic-random-access memory, for example. Assembly 100 includes a substrate 212. The term "substrate," as used herein, encompasses a semiconductor wafer as well as structures having one or more insulative, conductive, or semiconductive layers and materials. Thus, for example, the term embraces silicon-on-insulator, silicon-on-sapphire, and other advanced structures.

Substrate 212 supports a number of integrated elements 214, for example transistors 214a and 214b. Transistors 214a and 214b are covered by a mask layer 216, which, for example, comprises photoresist. In the exemplary embodiment, the transistors are metal-oxide-semiconductor field-effect transistors (MOSFETs); however, in other embodiments, the transistors are other types of field-effect transistors or bipolar junction transistors, or mixed transistor types. Still other embodiments use other types of integrated devices.

Layer 216 includes two exemplary via holes 216a and 216b positioned over respective contact regions (not shown) of transistors 214a and 214b and a trench 216c connecting the via holes. The exemplary embodiment forms layer 216 from photoresist, through use of spincoating, lithography, and photoresist remover. Some embodiments use plasma ashing to pattern the photoresist. Also, in the exemplary embodiment, via holes 216a and 216b are cylindrical with diameters of about 1000 nanometers and depths of about 500 nanometers. Trench 216c is less than 0.50 microns wide and at least one micron deep. The invention, however, is not limited to any particular mask material, formation technique, geometry, or dimensions.

Figure 2 shows that the exemplary method next forms a conductive structure 218 on mask 216, with one or more portions of the conductive structure contacting one or more exposed portions of the transistors. In the exemplary embodiment, this entails depositing a 20-30-nanometer-thick copper-, silver-, or gold-based seed layer (not shown separately) using a chemical-vapor-deposition, ionized-magnetron sputtering technique, or DC magnetron self-sputtering technique, and then electroplating additional copper-, silver-, or gold-based material on the seed layer to a total thickness of, for example, 0.5 microns. (As used herein, a copper-, silver-, or gold-based material includes at least 25 weight-percent of the base material.) An exemplary chemical-vapor-deposition technique follows a procedure such as that described in Y. Senzaki, "Chemical Vapor Deposition of Copper Using a New Liquid Precursor with Improved Thermal Stability," MRS Conference Proceedings of Advanced Metallization and Interconnect Systems for ULSI Applications in 1997, ULSI XIII, P. 451-455, 1998, which is incorporated herein by reference. This

procedure yields copper films at a typical deposition rate of 150-170 nanometers per minute at wafer temperatures of 195-225°C. The resistance of these films is in the range of 2.0 micro-ohm-centimeter after annealing at 400°C for five minutes.

Exemplary ionized sputtering technique and d-c magnetron sputtering techniques follow procedures similar to those outlined in S. M. Rossnagel et al., Metal Ion Deposition from Ionized Magnetron Sputtering Discharge," J. Vac. Sci. Technology B, 12(1), p. 449-453, 1994. And Z. J. Radzimski et al, "Directional Copper Deposition using D-C Magnetron Self-sputtering," J. Vac. Sci Technology B 16(3), p. 1102-1106, 1998. Exemplary conditions for the ionized-magnetron sputtering operation are: target power range of 10-30 kilowatts for a 200-300 millimeter diameter wafer (or integrated-circuit assembly), RF coil power at 3-5 kilowatts, negative DC bias of 100-200 volts, sputtering argon gas pressurized at 1-35 millitorrs. Ionized-magnetron sputtering, which provides greater acceleration of the metal deposition material than conventional sputtering, forces the sputtered material to more closely conform to the interior profiles of holes and trenches of the targeted surface.

Notably, the exemplary embodiment omits formation of an adhesion layer to promote adhesion of copper (or other materials) to the mask layer. Some embodiments use a 20-50 nanometer-thick layer of titanium nitride (TiN) over the transistor contacts as an adhesion layer and a diffusion barrier. However, other embodiments provide an adhesion layer of titanium nitride. After depositing the conductive material, the exemplary method removes excess material, for example, using a chemical-mechanical planarization or polishing procedure.

Next, as Figure 3 shows, the exemplary method forms a mask layer 220 over conductive structure 218. Mask layer 220 includes an opening (via) 220a which exposes a portion of conductive structure 218 and a trench 220b which intersects opening 220a. Exemplary formation of conductive structure follows a procedure similar to that used to form mask layer 216 and occurs with at least a portion of mask layer 216 still in place.

Figure 4 shows that the exemplary method next forms a conductive structure 222 on mask 216, with portions of structure 222 contacting exposed portions of conductive structure 218. In the exemplary embodiment, this entails depositing a 20-30-nanometer-thick copper-, silver-, or gold-based seed layer and electroplating additional copper-, silver-, or gold-based material to an exemplary thickness of 0.5 microns. Excess material is then removed using a chemical-mechanical planarization or polishing procedure. Subsequently, one or more higher-level conductive structures can be formed similarly.

Figure 5 shows that after forming conductive structure 222, the method removes at least a portion of mask structures 216 and 220, defining one or more spaces or voids 224 around conductive structures 218 and 222. Without the surrounding masks, conductive structures 218 and 222 appears as a two-level airbridge. The exemplary embodiment removes substantially all of the mask structures by ashing them in an oxygen plasma.

After removal of the mask structures, the exemplary method forms a diffusion barrier 226 on at least portions of conductive structures 218 and 222. In the exemplary embodiment, this entails growing or depositing a two-to-six nanometer-thick layer of WSiN over substantially all of conductive structures 218 and 222. Exemplary formation of this layer of WSiN occurs within a hybrid reaction chamber such as that described in co-filed and co-assigned patent application entitled Methods and Apparatus for Making Copper Wiring in Integrated Circuits. This application, attorney docket 303.618US1 (99-0469), is incorporated herein by reference.

More particularly, exemplary formation of diffusion barrier 226 entails forming a graded composition of tungsten silicide (WSi_x), with x varying from 2.0 to 2.5. This entails heating the assembly to a temperature of 360°C and introducing hydrogen, tungsten hexafluoride, and silane gases into a process chamber enclosing the assembly. The exemplary embodiment introduces the hydrogen and tungsten hexaflouride gases about one-to-three seconds before introducing the silane gas and stops introducing the silane gas about one-to-three seconds before stopping

introduction of the hydrogen and tungsten hexaflouride. Exemplary flow rates for the silane and tungsten hexaflouride gases are respectively 1000 sccm and 14 sccm. These flow rates result in a composition of $WSi_{2.3}$, with a growth rate of approximately 50 nanometers per minute.

To complete the diffusion barrier, the exemplary method nitrides the graded composition of WSi_x, forming WSi_xN_y. The exemplary nitridation follows an electron-cyclotron-resonance (ECR) plasma nitridation procedure. One version of this procedure is described in A. Hirata et al., WSiN Diffusion Barrier Formed by ECR Plasma Nitridation for Copper Damascene Interconnection, Extended Abstracts of 1998 International Conference on Solid State Devices and Materials, p. 260-261, which is incorporated herein by reference. This entails introducing nitrogen gas and argon gas into the chamber, with the argon gas exciting a plasma. In the exemplary embodiment, the WSi_xN_y is not a compound-forming barrier, but a stuffed barrier, which prevents diffusion by stuffing nitrogen atoms into diffusion paths, such as interstitial sites, within the tungsten silicide. Other embodiments uses diffusion barriers having different compositions and thicknesses, and some entirely omit a diffusion barrier.

Figure 7 shows that after completion of diffusion barrier 226, the exemplary method fills at least a portion of the remainder of space 224 (denoted 224' in Figure 6) with one or more insulative materials. The exemplary embodiment fills substantially all of space 224, which was previously occupied by mask structures 216 and 220, with a single dielectric material using a single procedure. More particularly, the exemplary embodiment vapor deposits a silicon oxide, such as SiO_2, or low-k (that is, low-dielectric-constant) materials, such as xerogels or aerogels. Various methods, such as physical-vapor deposition, chemical-vapor deposition, spin-coating, sol-gel procedures, and so forth can be used to apply these dielectrics.

Figure 8 shows one example of the unlimited number of applications for one or more embodiments of the present invention: a generic integrated memory circuit 600. Circuit 600, which operates according to well-known and understood

principles, is generally coupled to a processor (not shown) to form a computer system. More precisely, circuit 600 includes a memory array 642 which comprises a number of memory cells 643a-643d, a column address decoder 644, and a row address decoder 645, bit lines 646, word lines 647, and voltage-sense-amplifier circuit 648 coupled to bit lines 646.

In the exemplary embodiment, each of the memory cells, the address decoders, and the amplifier circuit includes one or more copper-, silver, or gold-based conductors according to the present invention. Other embodiments, use conductors of other materials, made in accord with one or more methods of the present invention. In addition, connections between the address decoders, the memory array, the amplifier circuit are implemented using similar interconnects.

Conclusion

In furtherance of the art, the inventors have one or more exemplary methods for making integrated-circuit wiring from materials, such as copper-, silver-, and gold-based metals, some of which allow fabrication of wiring with fewer steps and lower electrical resistance than some conventional methods. One exemplary method initially forms a first mask and a first metal structure on the first mask and then forms a second mask and a second metal structure on the second mask, with the first mask and first metal structure still in place. Continuing, this exemplary method removes both masks in a single removal procedure, forms a diffusion barrier to both metal structures in a single formation procedure, and fills insulative material in and around both metal structures in a single fill procedure. Applying one or more procedures across multiple wiring levels, as in this embodiment, ultimately precludes the necessity of applying these procedures separately to each wiring level and thus promises to simplify fabrication.

The embodiments described above are intended only to illustrate and teach one or more ways of practicing or implementing the present invention, not to restrict its breadth or scope. The actual scope of the invention, which embraces all ways of

practicing or implementing the invention, is defined only by the following claims and their equivalents.

Claims

1. A method of making integrated circuits, comprising:

forming a first mask layer having one or more openings or trenches, with each opening exposing a portion of one or more transistor contact regions;

forming a first conductive structure on the first mask layer, with the first conductive structure having one or more portions contacting at least one of the exposed transistors contact regions;

forming a second mask layer having one or more openings or trenches, with each opening exposing a portion of the first conductive structure;

forming a second conductive structure on the second mask layer, with one or more portions of the second conductive structure contacting at least one of the exposed portions of the first conductive structure;

removing in a single procedure at least respective portions of the first and second mask structures after forming the second conductive structure;

forming in a single procedure a diffusion barrier on at least respective portions of the first and second conductive structures after removing at least the respective portions of the first and second mask structures; and

forming in a single procedure an insulator on and between the first and second conductive structures after forming the diffusion barrier.

2. The method of claim 1:

wherein forming the first and second mask layers comprises depositing photoresist; and

wherein forming the first and second conductive structures comprises filling one or more of the openings or trenches with a copper-, silver-, or gold-based material.

3. The method of claim 1:

wherein removing the first and second mask layers comprises ashing the first and second mask layers;

wherein forming the insulator on and between the first and second conductive structures comprises spin-coating the first and second conductive structures with an aerogel or xerogel.

4. A method of making integrated circuits, comprising:

a step for forming a first mask layer having one or more openings or trenches, with each opening exposing a portion of one or more transistor contact regions;

a step for forming a first conductive structure on the first mask layer, with the first conductive structure having one or more portions contacting at least one of the exposed transistors contact regions;

a step for forming a second mask layer having one or more openings or trenches, with each opening exposing a portion of the first conductive structure;

a step for forming a second conductive structure on the second mask layer, with one or more portions of the second conductive structure contacting at least one of the exposed portions of the first conductive structure;

a step for removing concurrently at least respective portions of the first and second mask structures after forming the second conductive structure;

a step for forming a diffusion barrier on at least respective portions of the first and second conductive structures after removing at least the respective portions of the first and second mask structures; and

a step for forming an insulator on and between the first and second conductive structures after forming the diffusion barrier.

5. A method comprising:

forming a conductive structure;

forming a diffusion-barrier lining around the conductive structure after forming the conductive structure; and

forming an insulative structure around the conductive structure after forming the diffusion-barrier lining.

6. The method of claim 5, wherein forming the conductive structures comprises applying a copper-, silver-, or gold-based material.

7. The method of claim 5, wherein forming the conductive structure comprises:

ionized sputtering or DC magnetron sputtering of a copper-based material onto at least a portion of the diffusion barrier; and

electroplating a copper-based material onto the sputtered copper-based material.

8. The method of claim 5, wherein forming the insulative structure comprises spin-coating an aerogel or xerogel.

9. The method of claim 5, wherein forming the diffusion-barrier lining comprises forming a graded composition of WSi_x, where x varies from 2.0 to 2.5.

10. The method of claim 5, wherein forming the diffusion-barrier lining comprises:

forming a graded composition of WSi_x, where x varies from 2.0 to 2.5; and

nitriding the graded composition of WSi_x.

11. The method of claim 5 wherein nitriding the graded composition of WSi_x comprises exciting a plasma with argon gas.

12. The method of claim 5, wherein forming the diffusion-barrier lining comprises:

introducing tungsten hexaflouride and hydrogen gases into a wafer processing chamber for a predetermined amount of time;

introducing silane gas into the chamber a first predetermined time after introducing the tungsten hexaflouride gas; and

terminating introduction of the silane gas a second predetermined time before terminating introduction of the tungsten hexaflouride and hydrogen gases into the chamber.

13. The method of claim 5, wherein the first and second times are in the range of about one to about three seconds.

14. A method comprising:

a step for forming a conductive structure;

a step for forming a diffusion-barrier lining around the conductive structure after forming the conductive structure; and

a step for forming an insulative structure around the conductive structure after forming the diffusion-barrier lining.

15. A method comprising:

forming a first mask in an integrated-circuit assembly;

forming a first conductor on the first mask;

forming a second mask on the first conductor;

forming a second conductor on the second mask; and

removing at least respective portions of the first and second masks in a single material-removal procedure.

16. The method of claim 15, wherein removing at least respective portions of the first and second mask in the single material-removal procedure comprises removing substantially all of the first and second masks.

17. The method of claim 15, wherein removing at least respective portions of the first and second masks comprises ashing the first and second masks.

18. The method of claim 15, wherein forming the first mask and forming the second mask each comprise applying a photoresist to a surface in the integrated circuit assembly using spincoating.

19. The method of claim 15, wherein forming the first conductor or forming the second conductor comprises applying a copper-, silver-, or gold-based material to a surface in the integrated-circuit assembly.

20. The method of claim 15, wherein forming the first conductor comprises:
ionized sputtering or DC magnetron sputtering of a copper-based material onto at least a portion of the diffusion barrier; and
electroplating copper-based material onto the sputtered copper-based material.

21. A method comprising:
a step for forming a first mask in an integrated-circuit assembly;
a step for forming a first conductor on the first mask;
a step for forming a second mask on the first conductor;
a step for forming a second conductor on the second mask; and
a step for removing respective portions of at least the first and second mask in a single material-removal procedure.

22. A method comprising:

forming a first wiring level in an integrated circuit assembly;

forming a second wiring level in the integrated circuit assembly, the second wiring level electrically coupled to the first wiring level; and

forming a diffusion barrier around at least a portion of the first wiring level and at least a portion of the second wiring level in a single barrier-formation procedure.

23. The method of claim 22, wherein forming the first wiring level or forming the second wiring level comprises applying a copper-, silver-, or gold-based material to a surface in the integrated-circuit assembly.

24. The method of claim 22, wherein the first wiring layer includes one or more first substantially planar portions and the second wiring layer includes one or more second substantially planar portions which are substantially parallel to the first substantially planar portions.

25. The method of claim 22, wherein forming the first wiring layer comprises:

ionized sputtering or DC magnetron sputtering of a copper-based material onto at least a portion of the diffusion barrier; and

electroplating copper-based material onto the sputtered copper-based material.

26. The method of claim 22, wherein forming the diffusion-barrier lining comprises:

introducing tungsten hexaflouride and hydrogen gases into a wafer processing chamber for a predetermined amount of time;

introducing silane gas into the chamber a first predetermined time after introducing the tungsten hexaflouride gas; and

terminating introduction of the silane gas a second predetermined time before terminating introduction of the tungsten hexaflouride and hydrogen gases into the chamber.

27. A method comprising:
forming a first wiring level in an integrated circuit assembly;
forming a second wiring level in the integrated circuit assembly; and
forming a diffusion barrier around at least a portion of the first wiring level and at least a portion of the second wiring level in a single barrier-formation procedure.

28. The method of claim 27, further comprising:
forming a third wiring level in the integrated-circuit assembly after forming the second wiring level, wherein forming the diffusion barrier in the single barrier-formation procedure forms at least a portion of the includes insulative structure occurs after forming the first, second, and third wiring levels.

29. A method comprising:
a step for forming a first wiring level in an integrated circuit assembly;
a step for forming a second wiring level in the integrated circuit assembly; and
a step for forming a diffusion barrier around at least a portion of the first wiring level and at least a portion of the second wiring level in a single barrier-formation procedure.

30. A method comprising:
forming a first wiring level in an integrated-circuit assembly;
forming a second wiring level in the integrated-circuit assembly; and

forming an insulative structure having at least a portion between the first and second wiring levels after forming the second wiring level.

31. The method of claim 30, further comprising:

forming a third wiring level in the integrated-circuit assembly after forming the second wiring level, wherein forming the insulative structure occurs after forming the first, second, and third wiring levels.

32. A method comprising:

forming a first structure having one or more trenches or openings;

forming a conductive structure in at least one of the trenches or openings;

removing substantially all of the first structure to define a space around the conductive structure;

applying a diffusion-barrier material to at least a portion of the conductive structure after removing substantially all of the first structure;

forming an insulative structure on at least a portion of the diffusion-barrier material applied to the conductive structure.

33. A method comprising:

forming a non-conductive structure having one or more trenches or openings;

forming a conductive structure in at least one of the trenches or openings;

removing substantially all of the non-conductive structure to define a space around the conductive structure;

applying a diffusion-barrier material to at least a portion of the conductive structure after removing substantially all of the non-conductive structure;

forming an insulative structure on at least a portion of the diffusion-barrier material applied to the conductive structure.

34. The method of claim 33, wherein the diffusion-barrier material contacts a surface of the conductive structure.

35. A method of making integrated circuits, comprising:

providing a layer including one or more transistors, with each transistor having one or more transistor contact regions;

forming a first mask layer having one or more openings, with each opening exposing at least a portion of at least one of the transistor contact regions;

forming a first conductive structure over the first mask layer and contacting one or more of the transistor contact regions;

forming a second mask layer having one or more openings, with each opening exposing at least a portion of the first conductive structure;

forming a second conductive structure over the second mask layer, with the second conductive structure contacting one or more exposed portions of the first conductive structure;

removing substantially all of the first and second mask structures after forming the second conductive structure;

forming a diffusion barrier on least the first and second conductive structures after removing substantially all of the first and second mask structures;

forming an insulative material between at least a portion of the first conductive structure and at least a portion of the second conductive structure after removing substantially all of the first and second mask structures.

36. A method of making an integrated memory circuit, comprising:

forming a first mask layer having one or more openings or trenches, with each opening exposing a portion of one or more transistor contact regions;

forming a first gold-based conductive structure on the first mask layer, with the first gold-based conductive structure having one or more portions contacting at least one of the exposed transistors contact regions;

forming a second mask layer having one or more openings or trenches, with each opening exposing a portion of the first conductive structure;

forming a second gold-based conductive structure on the second mask layer, with one or more portions of the second gold-based conductive structure contacting at least one of the exposed portions of the first gold-based conductive structure;

removing in a single procedure at least respective portions of the first and second mask structures after forming the second gold-based conductive structure;

forming in a single procedure a diffusion barrier on at least respective portions of the first and second gold-based conductive structures after removing at least the respective portions of the first and second mask structures; and

forming in a single procedure an insulator on and between the first and second gold-based conductive structures after forming the diffusion barrier.

37. The method of claim 36:

wherein forming the first and second mask layers comprises depositing photoresist;

wherein removing the first and second mask layers comprises ashing the first and second mask layers; and

wherein forming the insulator on and between the first and second conductive structures comprises spin-coating the first and second gold-based conductive structures with an aerogel or xerogel.

38. A method of making an integrated memory circuit, comprising:

forming a first mask layer having one or more openings or trenches, with each opening exposing a portion of one or more transistor contact regions;

forming a first silver-based conductive structure on the first mask layer, with the first silver-based conductive structure having one or more portions contacting at least one of the exposed transistors contact regions;

forming a second mask layer having one or more openings or trenches, with each opening exposing a portion of the first conductive structure;

forming a second silver-based conductive structure on the second mask layer, with one or more portions of the second silver-based conductive structure contacting at least one of the exposed portions of the first silver-based conductive structure;

removing in a single procedure at least respective portions of the first and second mask structures after forming the second silver-based conductive structure;

forming in a single procedure a diffusion barrier on at least respective portions of the first and second silver-based conductive structures after removing at least the respective portions of the first and second mask structures; and

forming in a single procedure an insulator on and between the first and second silver-based conductive structures after forming the diffusion barrier.

39. The method of claim 38:

wherein forming the first and second mask layers comprises depositing photoresist;

wherein removing the first and second mask layers comprises ashing the first and second mask layers; and

wherein forming the insulator on and between the first and second conductive structures comprises spin-coating the first and second silver-based conductive structures with an aerogel or xerogel.

40. A method of making an integrated memory circuit, comprising:

forming a first mask layer having one or more openings or trenches, with each opening exposing a portion of one or more transistor contact regions;

forming a first copper-based conductive structure on the first mask layer, with the first copper-based conductive structure having one or more portions contacting at least one of the exposed transistors contact regions;

forming a second mask layer having one or more openings or trenches, with each opening exposing a portion of the first conductive structure;

forming a second copper-based conductive structure on the second mask layer, with one or more portions of the second copper-based conductive structure contacting at least one of the exposed portions of the first copper-based conductive structure;

removing in a single procedure at least respective portions of the first and second mask structures after forming the second copper-based conductive structure;

forming in a single procedure a diffusion barrier on at least respective portions of the first and second copper-based conductive structures after removing at least the respective portions of the first and second mask structures; and

forming in a single procedure an insulator on and between the first and second copper-based conductive structures after forming the diffusion barrier.

41. The method of claim 40:

wherein forming the first and second mask layers comprises depositing photoresist;

wherein removing the first and second mask layers comprises ashing the first and second mask layers; and

wherein forming the insulator on and between the first and second conductive structures comprises spin-coating the first and second copper-based conductive structures with an aerogel or xerogel.

42. An integrated-memory-circuit assembly comprising:

a surface having one or more transistor regions;

a first copper-, silver-, or gold-based wiring level having one or more first portions coupled to one or more of the transistors, the one or more first portions having a first diffusion-barrier lining and defining a substantially horizontal first plane, with the first plane and the surface defining a first open region; and

at least a second copper-, silver-, or gold-based wiring level having one or more second portions electrically coupled and attached to the first gold-based wiring level, the one or more second portions having a second diffusion-barrier lining and defining a substantially horizontal second plane which is substantially parallel to the first plane, with the first and second planes defining a second open region.

Abstract of the Disclosure

Integrated circuits, the key components in thousands of electronic and computer products, include interconnected networks of electrical components. The components are typically wired, or interconnected, together with aluminum wires. In recent years, researchers have begun using copper instead of aluminum to form integrated-circuit wiring, because copper offers lower electrical resistance and better reliability at smaller dimensions. However, copper typically requires use of a diffusion barrier to prevent it from contaminating other parts of an integrated circuit. Unfortunately, typical diffusion barrier materials add appreciable resistance to the copper wiring, and thus negate some advantages of using copper. Moreover, conventional methods of forming the copper wiring are costly and time consuming. Accordingly, the inventors devised one or more exemplary methods for making integrated-circuit wiring from materials, such as copper-, silver-, and gold-based metals. One exemplary method removes two or more masks in a single removal procedure, forms a low-resistance diffusion barrier on two or more wiring levels in a single formation procedure, and fills insulative material around and between two or more wiring levels in a single fill procedure. This and other embodiments hold the promise of simplifying fabrication of integrated-circuit wiring dramatically.

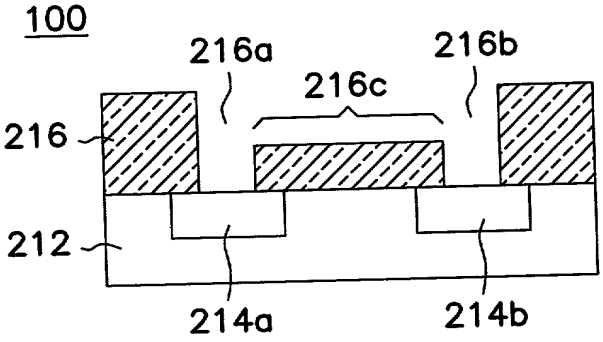

FIG. 1

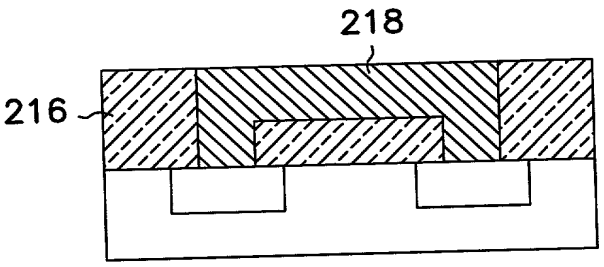

FIG. 2

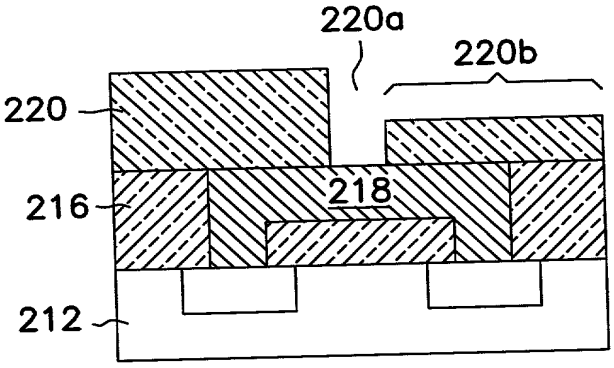

FIG. 3

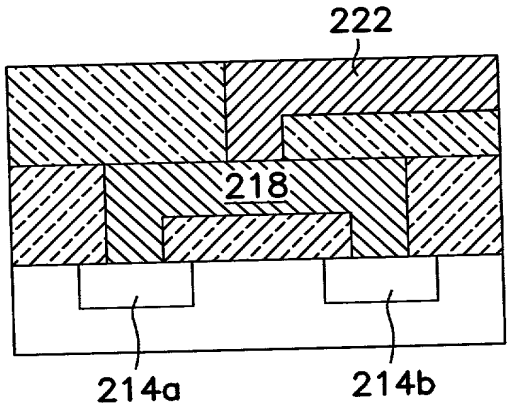

FIG. 4

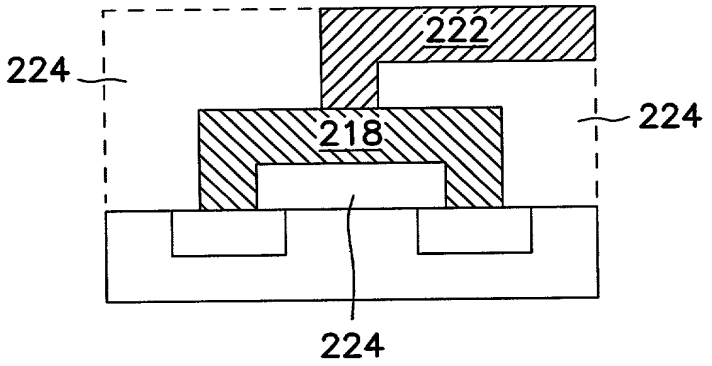

FIG. 5

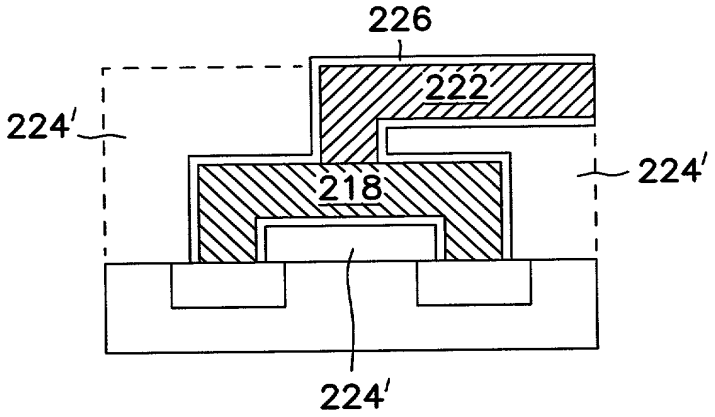

FIG. 6

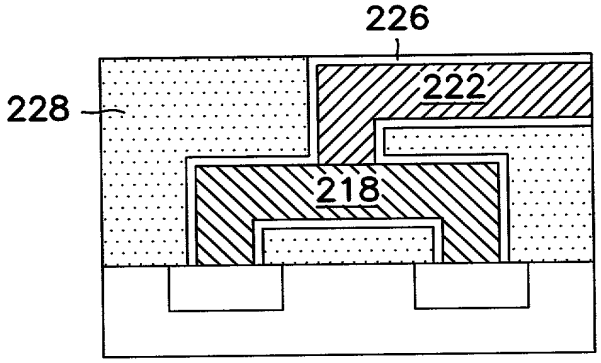

FIG. 7

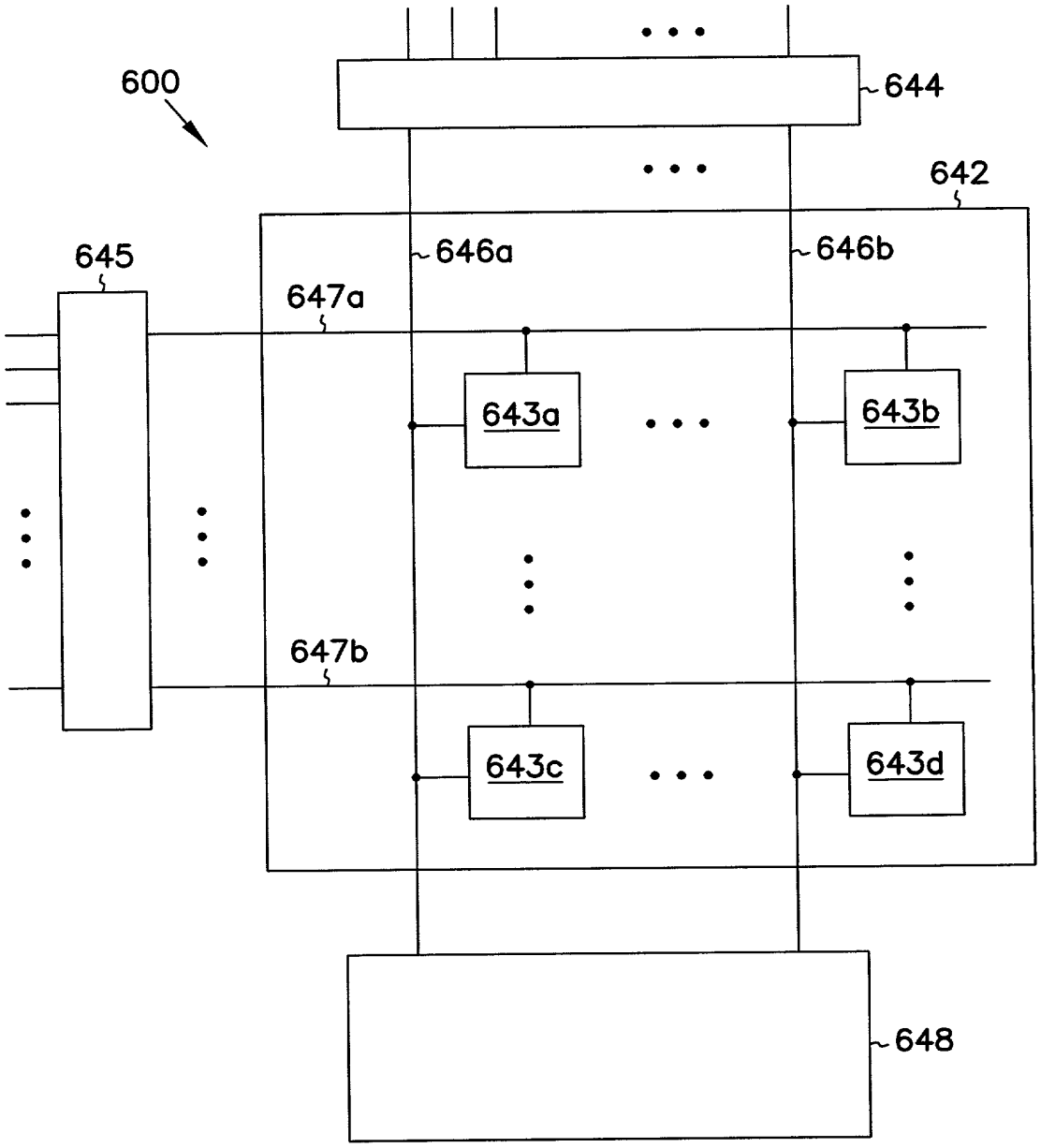

FIG. 8

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

DECLARATION FOR PATENT APPLICATION

As a below named inventor I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am an original, first an joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHODS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS .

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

No such claim for priority is being made at this time.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application.

No such claim for priority is being made at this time.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of joint inventor number 1 : **Kie Y. Ahn**
Citizenship: **United States of America** Residence: **Chappaqua, NY**
Post Office Address: 639 Quaker St.
Chappaqua, NY 10514

Signature: Kie Y. Ahn Date: Dec. 10, 1999
Kie Y. Ahn

Full Name of joint inventor number 2 : **Leonard Forbes**
Citizenship: **United States of America** Residence: **Corvallis, OR**
Post Office Address: 965 NW Highland Terrace
Corvallis, OR 97330

Signature: _____ Date: _____
Leonard Forbes

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of joint inventor number 1 : **Kie Y. Ahn**
Citizenship: **United States of America** Residence: **Chappaqua, NY**
Post Office Address: 639 Quaker St.
Chappaqua, NY 10514

Signature: _____ Date: _____
Kie Y. Ahn

Full Name of joint inventor number 2 : **Leonard Forbes**
Citizenship: **United States of America** Residence: **Corvallis, OR**
Post Office Address: 965 NW Highland Terrace
Corvallis, OR 97330

Signature: _____ Date: 6 DEC 99
Leonard Forbes

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

---

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) it establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) it refutes, or is inconsistent with, a position the applicant takes in:

(i) opposing an argument of unpatentability relied on by the Office, or

(ii) asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

S/N Unknown **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Kie Y. Ahn et al.	Examiner: Unknown	
Serial No.:	Unknown	Group Art Unit: Unknown	
Filed:	Herewith	Docket: 303.648US1	
Title:	METHODS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS		

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Micron Technology, Inc., assignee of the entire right, title and interest in the above-identified application by assignment attached hereto, hereby appoints the attorneys and agents of the firm of SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A., listed as follows:

Adams, Gregory J.	Reg. No. 44,494	Huebsch, Joseph C.	Reg. No. 42,673	Nelson, Albin J.	Reg. No. 28,650
Anglin, J. Michael	Reg. No. 24,916	Jurkovich, Patti J.	Reg. No. 44,813	Nielsen, Walter W.	Reg. No. 25,539
Bianchi, Timothy E.	Reg. No. 39,610	Kalis, Janal M.	Reg. No. 37,650	Oh, Allen J.	Reg. No. 42,047
Billion, Richard E.	Reg. No. 32,836	Kaufmann, John D.	Reg. No. 24,017	Padys, Danny J.	Reg. No. 35,635
Black, David W.	Reg. No. 42,331	Klima-Silberg, Catherine I.	Reg. No. 40,052	Parker, J. Kevin	Reg. No. 33,024
Brennan, Leoniede M.	Reg. No. 35,832	Kluth, Daniel J.	Reg. No. 32,146	Peacock, Gregg A.	Reg. No. 45,001
Brennan, Thomas F.	Reg. No. 35,075	Lacy, Rodney L.	Reg. No. 41,136	Perdok, Monique M.	Reg. No. 42,989
Brooks, Edward J., III	Reg. No. 40,925	Leffert, Thomas W.	Reg. No. 40,697	Polglaze, Daniel J.	Reg. No. 39,801
Chu, Dinh C.P.	Reg. No. 41,676	Lemaire, Charles A.	Reg. No. 36,198	Prout, William F.	Reg. No. 33,995
Clark, Barbara J.	Reg. No. 38,107	Litman, Mark A.	Reg. No. 26,390	Schumm, Sherry W.	Reg. No. 39,422
Dahl, John M.	Reg. No. 44,639	Lundberg, Steven W.	Reg. No. 30,568	Schwegman, Micheal L.	Reg. No. 25,816
Drake, Eduardo E.	Reg. No. 40,594	Mack, Lisa K.	Reg. No. 42,825	Slifer, Russell D.	Reg. No. 39,838
Eliseeva, Maria M.	Reg. No. 43,328	Maki, Peter C.	Reg. No. 42,832	Smith, Michael G.	Reg. No. P-45,368
Embretson, Janet E.	Reg. No. 39,665	Malen, Peter L.	Reg. No. 44,894	Steffey, Charles E.	Reg. No. 25,179
Fogg, David N.	Reg. No. 35,138	Mates, Robert E.	Reg. No. 35,271	Terry, Kathleen R.	Reg. No. 31,884
Fordenbacher, Paul J.	Reg. No. 42,546	McCrackin, Ann M.	Reg. No. 42,858	Viksnins, Ann S.	Reg. No. 37,748
Forrest, Bradley A.	Reg. No. 30,837	Nama, Kash	Reg. No. 44,255	Woessner, Warren D.	Reg. No. 30,440
Harris, Robert J.	Reg. No. 37,346				

and also attorneys Michael L. Lynch (Reg. No. 30,871) and Lia M. Pappas (Reg. No. 34,095) of Micron Technology, Inc., as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The assignee certifies that the above identified assignment has been reviewed and to the best of the assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

Schwegman, Lundberg, Woessner & Kluth, P.A.
Attn: Eduardo E. Drake
P.O. Box 2938
Minneapolis, MN 55402

Telephone: (612) 349-9593
Facsimile: (612) 339-3061

Dated: Jan 6, 2000

MICRON TECHNOLOGY, INC.

By: _____

Name: Michael L. Lynch

Title: Chief Patent Counsel